

## Claims:

1. An apparatus having an electrostatic discharge (ESD) device, the ESD device comprising:

a voltage divider to provide a first intermediate voltage potential;

5 a first current sink transistor;

a second current sink transistor coupled in series with the first current sink transistor; and

a first drive circuit to provide an enabling voltage potential to the second current sink transistor, wherein the drive circuit comprises an inverter with an input coupled to receive the first intermediate voltage potential.

2. The apparatus of claim 1, wherein the first current sink transistor and the second current sink transistor are p-channel transistors.

3. The apparatus of claim 2, wherein the first current sink transistor and the second current sink transistor are formed in a same well in a semiconductor substrate.

4. The apparatus of claim 2, wherein the first current sink transistor and the second current sink transistor are formed in different wells in a semiconductor substrate.

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5. The apparatus of claim 1, wherein the ESD device further comprises:  
 a third current sink transistor coupled in series with the first current sink transistor; and  
 a second drive circuit to provide an enabling voltage potential to the third  
 5 current sink transistor.

6. The apparatus of claim 5, wherein the voltage divider is adapted to  
 provide a second intermediate voltage potential and the second drive circuit  
 comprises an inverter with an input coupled to receive the second intermediate  
 10 voltage potential

7. The apparatus of claim 1, wherein the voltage divider comprises at least  
 four transistors coupled in series that have substantially similar channel lengths.

8. The apparatus of claim 1, wherein the ESD device further comprises a  
 15 latch coupled to the voltage divider.

9. An apparatus comprising:

a static random access memory; and

an integrated circuit, the integrated circuit having an electrostatic protection circuit comprising:

- 5                   . a first tier including an RC timer and a first current sink transistor; and  
a second tier, wherein the second tier is coupled to the RC timer.

10. The apparatus of claim 9, further comprising a voltage divider coupled to the first tier and the second tier to provide an intermediate voltage potential.

11. The apparatus of claim 10, wherein the second tier includes an inverter having an input terminal coupled to receive the intermediate voltage potential.

12. The apparatus of claim 9, wherein the first tier includes an inverter having an input terminal coupled to the RC timer.

13. The apparatus of claim 12, wherein the RC timer includes a p-channel transistor and a capacitor.

14. The apparatus of claim 13, wherein the capacitor is connected to the input terminal of the inverter and is adapted to receive the intermediate voltage potential.

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15. The apparatus of claim 9, wherein the voltage divider comprises at least four transistors coupled in series.

5 16. The apparatus of claim 9, further comprising a latch coupled to the voltage divider.

17. The apparatus of claim 9, wherein the voltage divider comprises at least two transistors coupled in series between voltage potential rails.

18. The apparatus of claim 9, wherein the voltage divider comprises at least two transistors coupled in series between voltage potential rails.

18. A method of enabling an electrostatic discharge device comprising:  
 enabling a first tier and a second tier of the electrostatic discharge device  
 with an RC timer in the first tier.

5 19. The method of claim 18, further comprising providing an intermediate  
 voltage potential to the second tier with a voltage divider.

20. The method of claim 19, wherein providing an intermediate voltage  
 potential includes providing the intermediate voltage potential to an input terminal  
 of an inverter in the second tier.